MINIATURE 8-18 GHZ FOUR CHANNEL FREQUENCY CONVERTER

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ABSTRACT

A state-of-the-art 8-18 GHz Front End comprising four phase and amplitude matched Frequency Converters consisting of ten selectable 1 GHz wide sub-band channels has been developed. An Integrated Local Oscillator (LO) Distribution module consisting of five dielectric resonator oscillators (DRO) operating at 11, 12, 13, 14, 15 GHz provides the downconversion of the 8 - 18 GHz RF spectrum to a 2 - 3 GHz intermediate frequency range. The input noise figure of each converter module is 10 dB with an associated gain of 46 dB ±1 dB. The spurious-free dynamic range is greater than 47 dB. The DRO oscillator accuracy is ±5 PPM/°C over a temperature range of 0°C to 50°C. The downconverter utilizes a combination of MIC and MMIC components to obtain the state-of-the-art performance in a small volume of 1966 cubic centimeters.

INTRODUCTION

Advances in current state-of-the-art acousto-optical Bragg-cell receivers require higher spurious-free dynamic range coupled with wider instantaneous bandwidth, low noise figure, high gain and small volume. A capability to characterize time coincident signals over wide dynamic range and simultaneous coverage of multi-octave RF frequency spectrum is required. The downconverters reported in the literature [1,2] have limited dynamic range, and narrow instantaneous bandwidth.

This paper presents the development of a miniature four channel phase and amplitude matched frequency downconverter operating over 8 - 18 GHz. A spurious free dynamic range of greater than 47 dB with associated gain 46 ± 1 dB and noise figure of 10 dB has been obtained. The converters are phase and amplitude matched to 12 degrees rms and 2 dB rms, respectively. The frequency converter consists of 10 selectable 1 GHz wide sub-band channels covering the 8 - 18 GHz band. The LO distribution module consists of 5 selectable DRO's operating at 11, 12, 13, 14, and 15 GHz to provide high side and low side conversion to a 2 - 3 GHz intermediate frequency range.

This work was supported by Naval Research Laboratories, Washington, DC, Contract No. N00014-86-R-MC11. Anthony Spezio is the Technical Project Manager.

RECEIVER DESIGN SYSTEM CONCEPT

Figure 1 shows the block diagram of the four channel Frequency Converter. Each of the four channels is comprised of a two diode limiter circuit at the input to protect the LNA FET amplifiers from 100 watt peak pulses of 1 microsecond width at .1% duty cycle and 1 watt CW signals. The 8-18 GHz RF input signals are then split into two intermediate sub-bands of 8-13 GHz (low band) and 13-18 GHz (high band) by a PIN-diode SPDT switch. The low band path consists of an LNA amplifier, low-pass filter and SP5T low band switch filter circuit. The high band path consists of a high-pass filter, LNA amplifier and a SP5T high-band switch filter circuit. This unique feature of intermediate sub-band selection allows for artificially extending the second-order intermodulation performance over broader bandwidths through the use of low and high pass filters to reject harmonic and out-of-band signals prior to downconversion in the mixer. The two intermediate sub-band channels are then re-combined in a SPDT switch. A monolithic dual-gate FET distributed amplifier is incorporated following the channelizing circuitry. The flexible feature associated with the dual-gate FET amplifier allowed recovery of losses associated with the switch/filter circuitry and the more important advantage of implementing temperature compensation control via the control gate of the dual-gate FET. The system temperature variations in gain/loss varied approximately ±5 dB which was easily offset via a thermistor controlled bias input to the control gate. This control feature is integrated in a custom hybrid design with a special sequencing regulator circuit needed for proper MMIC biasing.

Downconverting of the RF signals to the 2-3 GHz IF frequencies is accomplished via a special, high-level mixer. Each mixer is screened for phase and amplitude matching of ±8° and ±1 dB, respectively. Following the mixer is an IF bandpass filter required for Lo leakage suppression and a 2-3 GHz IF amplifier. This amplifier provided the 45 dB of IF gain in conjunction with a +40 dBm third-order output intercept point required to meet the 46 ± 1 dB gain and the 47 dB of spurious-free dynamic range specifications for the entire frequency converter channel.

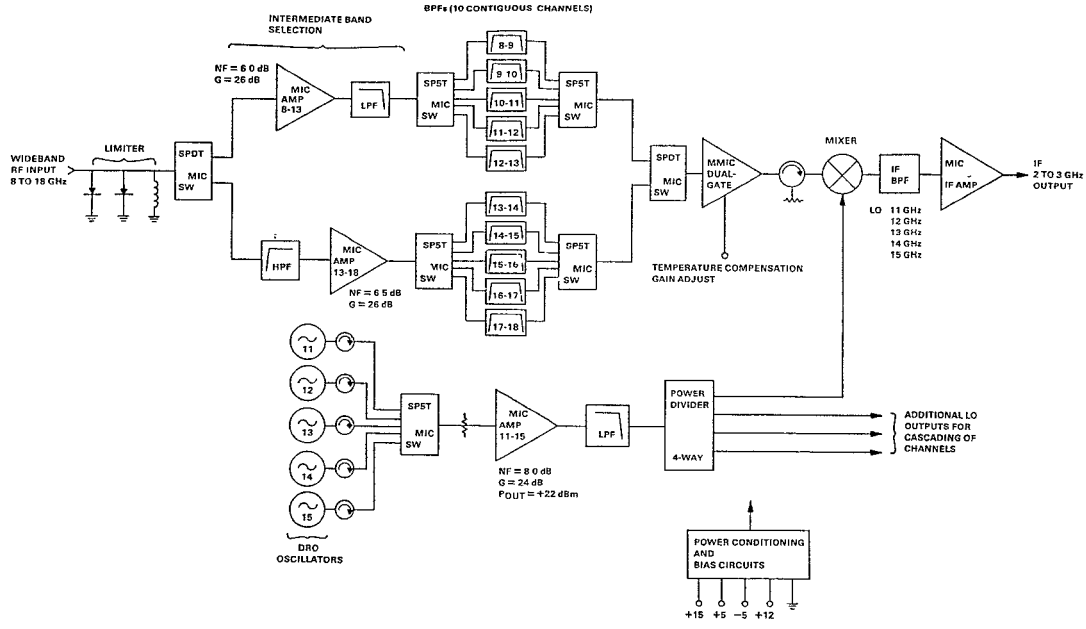

Figure 1. System Block Diagram of Four Channel Frequency Converter

The purpose of the LO distribution module is to generate the five stable frequencies to serve as the LO drive for the four-channel downconversion process. The method of generating the five selectable frequencies is shown in Figure 1. Five dielectric resonator oscillators (DRO) produce the frequencies 11, 12, 13, 14, and 15 GHz. The output power level from the LO distribution module is +15 dBm ±1 dB.

In the following sections a brief discussion of the design of the key components is presented.

LOW NOISE AMPLIFIER DESIGN

A balanced configuration for the low noise amplifiers is used. As discussed in the overall system performance section, the input frequency range of 8-18 GHz is divided into a low band 8-13 GHz and a high-band 13-18 GHz in order to extend the 2nd order response suppression. Therefore, the two individual amplifiers used are optimized in performance for each specific intermediate frequency range. The purpose of the LNA's is to establish the noise figure of the Front End channel consistent with a design goal of 10 dB. Additionally, tight control of the fabrication of the LNA's produced excellent phase and amplitude tracking from unit to unit. The maximum noise figure is 5 and 5.6 dB over the 8 - 18 and 13 - 18 GHz bands, respectively.

INTERMEDIATE BAND: HIGH-PASS AND LOW-PASS FILTERS DESIGN

The purpose of these two filters is to extend the second-order response suppression through attenuation of the out-of-band tones and harmonically generated tones created by the LNA's. The low-pass filter positioned after the low band LNA provides attenuation of the second harmonics of frequency in the 8 to 13 GHz range. The design is a ninth-order elliptic function filter, producing 40 dB minimum attenuation of harmonic signals greater than or equal to 16 GHz.

The high-pass filter positioned prior to the high band LNA suppresses low band signals. This filter is a seventh-order elliptic function design capable of providing 40 dB minimum attenuation of signals below 9 GHz.

Both filter circuits are implemented in microstrip using a combination of lumped-element and distributed equivalent geometries to realize the filter structures.

SWITCH/FILTER DESIGN

The switch filter establishs an instantaneous bandwidth of 1 GHz in ten contiguous channels from 8 to 18 GHz. Ten bandpass filters are contained between four SP5T switches to provide the selection. The switches utilize a series/shunt PIN diode configuration. The overall insertion loss of the complete switch filter network is set at 8.5 dB ±.5 dB. Two factors came into play in normalizing the insertion loss from channel to channel. The interconnecting transmission lines for the lower frequency filters are intentionally lengthened. Drop in thick film attenuator chips are then used to compensate the gain (loss) from channel to channel. Phase adjustment circuitry is also employed to compensate for phase variation due to manufacturing repeatability. The concept is implemented through the use of trombone line

adjustment structures. Typical channel to channel switch isolation are greater than 70 dB of the 8-18 GHz frequency range. The driver circuitry used are a custom hybrid design switch/driver designed for bi-polar outputs and low-power consumption.

The bandpass filter structures selected are 0.1 dB ripple, 5th order parallel-coupled line filters [5] implemented on 25 mil and 15 mil alumina substrate. The filter selectivity is derived from the converter spurious-free dynamic range specification of 47 dB as it related to Image Frequency and LO rejection requirements.

DUAL GATE MMIC AMPLIFIER/ TEMPERATURE COMPENSATION CIRCUIT DESIGN

Since component temperature variations of the system yield a +3, -7 dB gain variation over the 0°C to 50°C operational temperature range, it is necessary to incorporate temperature compensation to offset these variations and maintain a tight overall system gain response of 46 dB ±1 dB. The temperature compensation is accomplished via the dual-gate FET monolithic distributed amplifier and a simple thermistor controlled bias input to the control gate of the dual-gate FET. An RT42 series thermistor is selected to provide linear resistance change with temperature. This thermistor is connected in a voltage-divider configuration. The sequencing is necessary to ensure that negative voltage is present prior to application of positive voltage for prevention of dual-gate FET burn-out. The dual gate FET amplifier selected for this application is the Texas Instruments Model TGA 8622 Distributed Dual Gate MMIC Amplifier chip. A gain variation of 0.03 dB/°C for the MMIC itself is included in the total system temperature variation calculation.

DRO OSCILLATOR DESIGN

A common-source series feedback oscillator configuration is selected to provide optimum temperature stability (±5 PPM/°C) with no spurious oscillations. This configuration provides the most gain and therefore supplies the maximum power output. The series-feedback in the source is capacitive and implemented through the use of an open-circuited transmission line. This design also utilizes an oscillator "turn-off" circuitry [4] implemented by coupling a PIN diode to the source self-bias circuit which produces a change in the S-parameter conditions for oscillation. A pre-determined bias current is applied through the pin diode producing an attenuated condition of the DRO to greater than 60 dB. The 60 dB of attenuation, along with the SP5T switch isolation, provides excellent attenuation of unselected LO feedthrough.

The dielectric resonators used as the frequency acquisition elements are from Trans Tech 8500 series. Resonator diameters and heights vary in accordance with the proper frequency at operation. Each oscillator is operated from an internally regulated +5V supply drawing approximately 30 mA of current.

LO DISTRIBUTION DESIGN

The five oscillator outputs are fed to SP5T PIN diode switch. The switch selects one of the five frequencies to present to the downconverter as the LO signal. Chip attenuators, inserted into the network between the oscillator and switch, ensure that the transient conditions of the switch do not pull the frequency of the oscillators. The selected frequency is then amplified to the proper level by an LO MIC amplifier. The output signal from the amplifier is fed to low-pass 7th order Chebyshev filter used to attenuate the second harmonic responses. The output signal is then distributed to the four outputs by single section four-way Wilkinson power divider circuit. The four simultaneous output levels present are +15 dBm ±1 dB over the temperature range of 0-50°C.

FABRICATION

The design of the Four Channel Frequency Converter is made up of five major subassemblies; four modularized downconverter assemblies and an LO distribution network. The assemblies contain a broad mixture of state-of-the-art technology that include MMIC and MIC amplifiers, DRO's, solid state mixers and switches, and phase, amplitude, and temperature compensating circuitry. The down-converter utilizes both soft microstrip and hard microstrip substrates as a transmission medium. The substrates are eutecticly attached to the carrier for optimum performance. The high power MESFET amplifiers have been located within the system to minimize the thermal impedance to the mounting plate.

THERMAL DESIGN CONSIDERATIONS

The power dissipation of the receiver is 117 Watts maximum. The thermal design considerations are driven by the requirement to minimize the thermal gradient between the mounting plate and the MESFET amplifiers. To achieve a minimal thermal impedance, the distance to the mounting plate is minimized and the cross sectional area of chassis is maximized. Thin module covers and dead air gaps aid in the eliminated "thermal cross talk" between adjoining modules. The down-converter is designed to meet all operational specifications over the temperature range of 0°C to 50°C when mounted on a 50°C cold plate.

EXPERIMENTAL RESULTS

The photographs of complete integrated assemblies of a single downconverter and LO distribution unit are shown in Figures 2 and 3, respectively. A photograph of the complete assembly of this phase and amplitude matched four-channel downconverter is shown in Figure 4. Figure 5 shows the actual measured performance of the channelized gain of the 8 - 18 GHz RF Input spectrum downconverted to the 2 - 3 GHz IF range. The horizontal sweep of the RF signal generator allows resolution of the individual channel conversion. The overall gain is 46 ±1 dB with noise figure less than 10 dB. The dynamic range of the downconverter is greater than 47 dB. The measured amplitude and phase tracking of the four

Figure 5 shows the actual measured performance of the channelized gain of the 8 - 18 GHz RF Input spectrum downconverted to the 2 - 3 GHz IF range. The horizontal sweep of the RF signal generator allows resolution of the individual channel conversion. The overall gain is 46 ±1 dB with noise figure less than 10 dB. The dynamic range of the downconverter is greater than 47 dB. The measured amplitude and phase tracking of the four channels is 2 dB RMS and 12 degrees RMS, respectively.

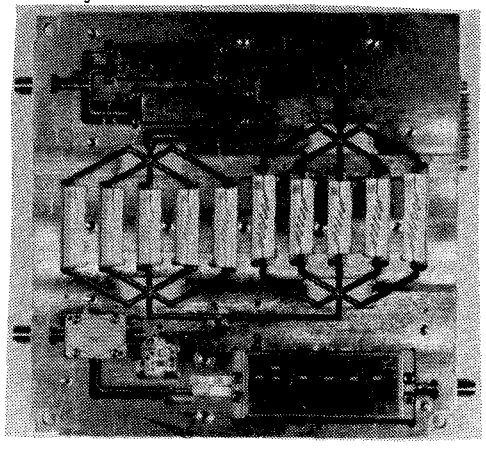

Figure 2. Single Downconverter Assembly

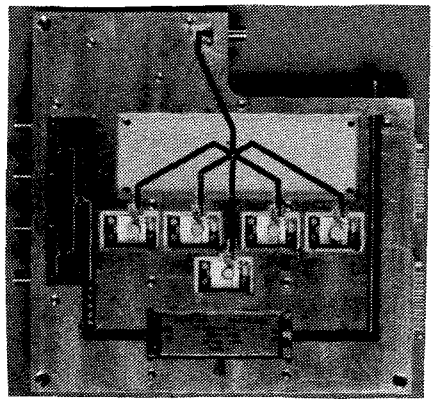

Figure 3. LO Distribution Unit

CONCLUSION

An 8-18 GHz four channel frequency down-converter has been presented. State-of-the-art performance has been obtained. The MIC channelized construction techniques have been utilized to substantially reduce the size and weight of the converter. A spurious free dynamic range of greater than 47 dB, noise figure of 10 dB with an associated gain of 46 ± 1 dB has been achieved over a mounting surface temperature range of 0°C to 50°C. An excellent phase and amplitude match of 12 degrees RMS and 2 dB RMS has been achieved between the four channels.

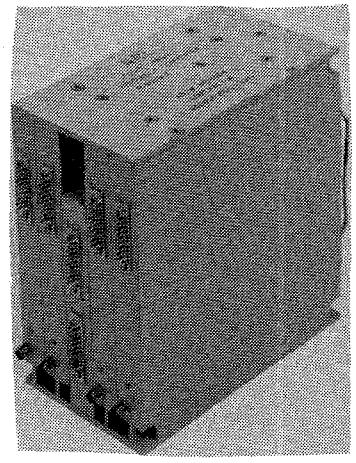

Figure 4. Complete Assembly for the Phase and Amplitude Matched Four Channel Frequency Converter

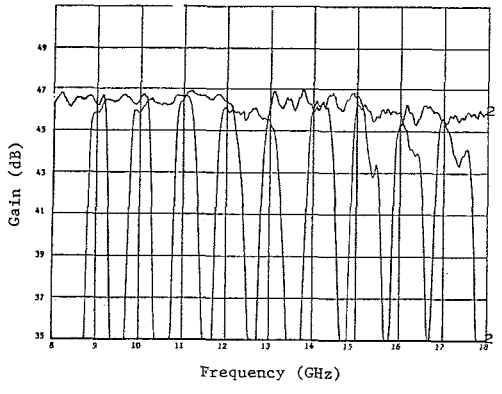

Figure 5. Channelized Gain Performance of a Single Downconverter

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ACKNOWLEDGEMENTS:

Authors would like to thank Anthony Spezio and Hal Levitt of Naval Research Laboratories, Washington, DC, for their technical direction and support of this program.